Amendments to the Claims

1. (CURRENTLY AMENDED) A circuit configuration for generating the drive signal of the deflection transistor of a cathode ray tube comprising a two-PLL system, characterized in that a delay block ~~(DB1)~~ is connected between the first and the second phase-locked loop. ~~(PLL1, PLL2).~~

2. (CURRENTLY AMENDED) A circuit configuration as claimed in claim 1, characterized in that the output ~~(HREF)~~ of the first phase-locked loop ~~(PLL1)~~ is connected to the input of the delay block ~~(DB1).~~

3. (CURRENTLY AMENDED) A circuit configuration as claimed in claim 1 ~~or 2~~, characterized in that the output of the first delay block ~~(DB1)~~ is connected to an input of the second phase-locked loop. ~~(PLL2).~~

4. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in claims 1 ~~to 3,~~ characterized in that the horizontal modulation ~~(hmod)~~ is a control value for the delay block. ~~(DB1).~~

5. (CURRENTLY AMENDED) A method as claimed in claim 4, characterized in that, together, the constant component ~~(const1)~~ of the target phase ~~(ZP1)~~ of the first phase-locked loop ~~(PLL1)~~ and the constant component ~~(const2)~~ of the first delay block ~~(DB1)~~ are greater than 100%.

6. (CURRENTLY AMENDED) A method as claimed in claim 4 ~~or 5~~, characterized in that the constant component ~~(const1)~~ of the first phase-locked loop PLL1 is 30%.

7. (CURRENTLY AMENDED) A method as claimed in claim 4 ~~any one of claims 4 to 6~~, characterized in that the constant component ~~(const2)~~ of the first delay block ~~(DB1)~~ is 80%.

8. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in claim 1 ~~any one of claims 1 to 3~~, characterized in that the target phase ~~(ZP3)~~ of the second phase-locked loop ~~(PLL2)~~ is constant.

9. (CURRENTLY AMENDED) A method as claimed in claim 8, characterized in that the target phase ~~(ZP3)~~ of the second phase-locked loop ~~(PLL2)~~ is 10%.

10. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in ~~any one of claims 1 to 3,~~ claim 1 characterized in that the dynamic component of the target phase ~~(ZP3)~~ of the second phase-locked loop ~~(PLL2)~~ is less than 20% of the entire horizontal modulation. ~~(hmod).~~

11. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in ~~any one of claims 1 to 3,~~ claim 1 characterized in that the dynamic component of the target phase (ZP3) of the second phase-locked loop (PLL2) is approximately 7% of the entire horizontal modulation (hmod).

12. (CURRENTLY AMENDED) A method of operating a circuit configuration, in particular a circuit configuration as claimed in ~~any one of claims 1 to 3,~~ claim 1 characterized in that the adjustment of the horizontal modulation ~~(hmod)~~ takes place in two parts ~~(hmod1 and hmod2),~~ wherein the first part (hmod1) is realized in the first delay block ~~(DB1),~~ and the second part ~~(hmod2)~~ is realized in the second phase-locked loop. ~~(PLL2).~~

13. (CURRENTLY AMENDED) A method as claimed in claim 12, characterized in that the first part ~~(hmod1)~~ realizes the larger component of the adjustment of the horizontal modulation ~~(hmod),~~ and the second part ~~(hmod2)~~ realizes the smaller component.

14. (CURRENTLY AMENDED) A method as claimed in claim 13, characterized in that the first part ~~(hmod1)~~ is 14% and the second part ~~(hmod2)~~ is 1%.

15. (CURRENTLY AMENDED) A method as claimed in ~~any one of claims 4 to 14,~~ claim 4 characterized in that the horizontal modulation ~~(hmod)~~ is 15%.

16. (CURRENTLY AMENDED) A method as claimed in ~~any one of claims 12 to 15,~~ claim 12 characterized in that the target phase ~~(ZP2)~~ for the first delay block ~~(DB1)~~ lies in a range from 66% to 94%, and the target phase ~~(ZP3)~~ for the second phase-locked loop ~~(PLL2)~~ lies in a range from 9% to 11%.

17. (CURRENTLY AMENDED) A method as claimed in ~~any one of claims 4 to 16,~~ claim 4 characterized in that the circuit configuration is implemented digitally.